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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	14

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/586,868	Applicant(s) CARUK ET AL.	
	Examiner Justin I. King	Art Unit 2111	

-- The MAILING DATE of this communication appears on th cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40* is/are allowed.

6)☒ Claim(s) *1-6,13,15,18-39 and 41-43* is/are rejected.

7)☒ Claim(s) *7-12, 14, 16-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The abstract is objected because it does not provide a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claim 41's second limitation, wherein the input buffer is operatively to receive the first internal signal from the first internal signal path must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 41-43 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not

described in the specification at the time the application was filed, had possession of the claimed invention. Claim 41's last limitation which states that the selector circuit is operatively coupled to the input buffer to provide the first internal signal from the first internal signal path to the first external signal path is not in the written description. As illustrated in the figure 5, the input buffer (structure 166) does not provide signals to the first external signal path. Claims 42-43 are rejected because they incorporate claim 41's limitations.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by Lane et al. (U.S. Patent No. 5,621,900).

Referring to claim 1: Lane discloses a first internal circuit (figure 1, structure 104) to provide a first internal signal via a first internal signal path (figure 1, structure 101), an input buffer (figure 1, structure 113) to received a first external signal via a first external signal path (figure 1, path between structures 112 and 113), and a selector circuit (figure 1, structure 107) coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal. Hence, the claim is anticipated by Lane.

7. Claims 1, 21-23, 25-27, 29-33, and 35-38 are rejected under 35 U.S.C. 102(a) as being anticipated by Melo et al. (U.S. Patent No 6,040,845).

Referring to claim 1: Melo discloses a first internal circuit (figure 1, structure 12) operable to provide a first internal signal via a first internal signal path (figure 1, structure CPU bus), an input buffer (figure 1, structure 24) operable to received a first external signal via a first external signal path (figure 1, path between structures 24 and 22), a selector circuit (figure 1, structure 14) coupled to the first internal circuit via the first internal signal path, and the input buffer, the selector circuit operable to select either the first internal signal or the first external signal. Hence, claim is anticipated by Melo.

Referring to claim 21: Melo discloses an internal circuit (figure 1, structure 12) receiving a bus bridge signal from an internal bus bridge (figure 1, structure 14), and an internal I/O circuit (figure 1, structure 28) arbitrating and controlling the signals from any external circuit (figure 1, structures 32a and 302b) from reaching the internal circuit; thus, Melo's internal I/O circuit preventing signals from any external circuit from reaching the internal circuit. Hence, claim is anticipated by Melo.

Referring to claim 22: Melo discloses that the external circuit (figure 2, structure 46) receives the bus bridge signal from the internal bus bridge; and the external circuit reflects the bus bridge signal to the internal I/O circuit (figure 2, structure 40).

Referring to claim 23: Melo discloses that the bus bridge has to arbitrate between the graphic signals and the peripheral master signals; thus, the signals been arbitrated and selected is the internal circuit signal, and therefore the bus receives an internal circuit signal from he

internal circuit and selects one of the internal circuit signal and the external circuit. Melo further discloses that the internal I/O circuit receives an external circuit signal from the external circuit (AGP), and the bus bridge also receives the external circuit signal once the arbiter receives and selects the signals.

Referring to claim 25: Melo's internal circuit does not have input buffer.

Referring to claim 26: Melo discloses the PCI bus/protocol.

Referring to claim 27: Melo discloses the AGP bus/protocol.

Referring to claim 29: Melo discloses a processing unit coupled to a processor bus (figure 1, structure CPU bus), a memory unit (figure 1, structure 18) coupled to a memory bus, and an integrated bus bridge graphics unit (figures 1-2, structure 14) coupled to the memory bus and further operably coupled to provide a signal to an external graphics bus (figures 1-2, AGP bus), the integrated bus bridge graphics unit comprises an internal circuit (figure 2, structure 44) controlling and arbitrating the signals from the external graphics bus, thus, it operably configured to avoid signals from the external graphics bus. Hence, the claim is anticipated by Melo.

Referring to claim 30: Melo discloses the integrated bus bridge graphics unit is operably coupled to receive a signal from the external graphics bus via an internal I/O circuit (figure 2, structure 40)

Referring to claim 31: Melo discloses that the bridge unit's arbiter (figure 2, structure 44) is configurable to select and to provide a signal to, one of the internal circuit and the external graphic bus, and further is operably to isolate the internal circuit from an external graphics bus signals while the arbiter not selecting the signals from the graphic bus signals.

Referring to claim 32: Melo discloses that the bridge is to select and to receive a signal from one of the internal circuit and external graphic bus (figure 1).

Referring to claim 33: Claim is rejected as the claim 31's argument above.

Referring to claim 35: Melo does not disclose any buffer between the bridge and the internal circuit.

Referring to claim 36: It is the selector's intended purpose to select signals that is uncorrupted by transmission line effects.

Referring to claim 37: Melo discloses the PCI protocol.

Referring to claim 38: Melo discloses the AGP protocol.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 2-5, 13, 15, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melo in view of Brickford et al. (U.S. Patent No. 6,141,021).

Referring to claim 2: Melo's disclosure is stated above, Melo does not explicitly disclose an output buffer and second internal signal path. Brickford discloses an output buffer (figure 6, structure 170) to receive a second internal signal (the signal from the AGP controller). Although Brickford does not explicitly disclose a separate second internal signal path for conveying signals into the output buffer, neither Brickford explicitly discloses the output buffer using the same first external signal path to transmit signals out, the court has held that duplication of the working parts of a device and forming in one piece an article which has formerly been formed in two pieces involve only routine skill in the art (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8 and Howard v. Detroit Stove Works, 150 U.S. 164). Such that it only takes routine skill in the computer art to add an additional internal signal path and to integrate the external output path and external input path into one external path. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Brickford's output buffer because it helps to enhance the smoothness of the signal transmitting in event that receiving device cannot accept the data as quick as the bus transmits.

Referring to claim 3: The signals in both Melo and Brickford's systems are transmitted via the bus and the associated bus protocol; hence, the signals are propagated with a common protocol.

Referring to claim 4: Melo discloses the PCI.

Referring to claim 5: Melo discloses the AGP.

Referring to claim 13: The circuit's connecting point to the bus is the bus interface.

Referring to claim 15: Claim 15 is rejected over the argument for claim 2 stated above.

Referring to claim 18: It is the selector's intended purpose to select signals that is uncorrupted by transmission line effects.

Referring to claim 19: Since Melo's input buffer is used by the graphics accelerator, the input buffer is inoperable to provide the external signal from the external circuit to the first internal circuit.

Referring to claim 20: Since the Melo's input buffer is used by the graphics accelerator, the input buffer is inoperable to provide the external signal from the external circuit to the first internal circuit. Furthermore, the output buffer is an internal buffer designed for conveying the internal signal to the external circuit, therefore, it is said that the output buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit.

11. Claims 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melo in view of Morris Mano's Computer System Architecture.

Referring to claim 24: Melo doses not explicitly disclose multiplexing for the selecting/arbitrating process. Mano's Computer System Architecture, as a popular academic textbook, teaches that it is known to use multiplexer for the selecting processing. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Mano onto Melo because Mano teaches one the fundamental computer structure in computer design.

12. Claims 6, 28, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melo in view of Applicant's admitted prior art the NGP protocol

Referring to claims 6, 28, and 39: Melo does not disclose the NGP protocol. As Applicant discloses in the spec, the NGP is a well-known industrial practice as an alternative to AGP and PCI at the time applicant made the invention. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt NGP onto Melo because NGP is a known alternative to the AGP and PCI in designing the computer structure.

13. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Melo in view of Chen et al. (U.S. Patent No. 5,850,530).

Referring to claim 34: Melo discloses that the integrated bus bridge isolates the external signal from the internal circuit (figure 1), but Melo does not explicitly disclose an input buffer for receiving the external signal. Chen discloses that it is known to equip the input buffer in the bridge (figures 1-2). Chen discloses that it is known to equip the input buffer to reduce the RETRY signal (columns 1-2). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Chen's bridge input buffer onto Melo's bridge because it can reduce the number of RETRY control signals, which will reduce the number of the arbitration attempts.

Allowable Subject Matter

14. Claims 7-12, 14, 16-17, and 40 contain allowable subject matter, and claim 40 is allowed.

15. The following is a statement of reasons for the indication of allowable subject matter:

Referring to claim 7: A configurable AGP interface circuit as structurally illustrated in figures 4 and 5 is structured to include a dedicated output buffer for outputting the internal signal to the add-in AGP card and this internal output signal does not go through the select circuit. The circuit is constructed in the structuring arrangement as the followings; a first internal circuit operable to provide a first internal signal via a first internal signal path; an input buffer operable to receive a first external signal via an first external signal path; and a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal; and an output buffer operative to receive a second internal signal via a second internal signal path and to provide the second internal signal via the first external signal path; and a second internal circuit operable to provide the second internal signal via the second internal signal path and to receive the selected signal via a third internal signal path, the selector circuit inoperable to receive the second internal signal; and the second internal circuit is operable to provide the second internal signal via the second internal signal path to both the first internal circuit and the output buffer.

Referring to claims 8-12 and 14: Claims are allowed because they incorporate the allowable subject matter from claim 7.

Referring to claim 16: A configurable AGP interface circuit as structurally illustrated in figures 4 and 5 is structured to include a dedicated output buffer for outputting the internal signal to the add-in AGP card and this internal output signal does not go through the select circuit. The circuit is constructed in the structuring arrangement as the followings; a configurable interface

circuit comprising: a first internal circuit operable to provide a first internal signal via a first internal signal path; an input buffer operable to receive a first external signal via an first external signal path; and a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal; a bus bridge, comprising a bus interface, operable to provide a second internal signal to the first internal circuit via a second internal signal path and to receive the selected signal via a third internal signal path, and an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

Referring to claim 17: Claim is allowed because it incorporates the allowable subject matter from claim 16.

Referring to claim 40: A configurable AGP interface circuit as structurally illustrated in figures 4 and 5 is structured to include a dedicated output buffer for outputting the internal signal to the add-in AGP card and this internal output signal does not go through the select circuit. The circuit is constructed in the structuring arrangement as the followings; an internal graphics controller operable to provide a first internal signal via a first internal signal path; an input buffer operable to receive a first external signal via an first external signal path; a selector circuit coupled to the internal graphics controller via the first internal sigh path and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal; a bus bridge comprising a bus interface operable to provide a second internal signal to the internal graphics controller via a second internal signal path and to receive

the selected signal via a third internal signal path; and an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

16. Claims 7-12 and 14 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action; and claims 7-12 and 14 are objected to as being dependent upon a rejected base claim, Applicant should rewrite them in independent form including all of the limitations of the base claim and any intervening claims.

17. Claims 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

18. A set of rejections is herein provided.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin King whose telephone number is (703) 305-4571. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephones are unsuccessfully, the examiner's supervisor, Mark Reinhart can be reached at (703) 308-3110.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose number is (703)-306-5631.

Justin King
February 6, 2004

XUAN M. THAI
PRIMARY EXAMINER
TC 2100